CVA date	26-5-2025

Part A. PERSONAL INFORMATION

Name and surname	Mª Luisa López Vallejo		
DNI/NIE/passport	13129154H	Edad	
Open Research and Contributor ID (ORCID)	0000-0002-3833-524X		

A.1. Current position

Institution	Universidad Politécnica de Madrid		
Dept./Center	Ingeniería Electrónica		
Address	ETSI Telecomunicación, Avda. Complutense 20, 28040 Madrid		
Phone number		e-mail	m.lopez.vallejo@upm.es
Prof. Category	Catedrática de Universidad	Fecha inicio	12-05-2016
UNESCO code	3307		
Key words	VLSI, Microelectronic Design, Circuits		

A.2. Education

PhD, Licensed, Graduate	University	Year
Ingeniero de Telecomunicación	Univ. Politécnica de Madrid	1992
Dr. Ingeniero de Telecomunicación	Univ. Politécnica de Madrid	1999

A.3. Scientific Quality Indicators

Sexenios de investigación: 6 (one is transfer). Date of the last one: Dec. 2023
Number of PhD supervised in the last 10 years: 9
Total cites: 1938 (Google Scholar)
Total number of publications (Q1): 31 h-index: 14 (WOS), 20 (Google Scholar)

Part B. CV SUMMARY

María Luisa López Vallejo is a Full Professor at the Universidad Politécnica de Madrid (UPM) in the Department of Electronic Engineering (ETSIT) and leads the Integrated Systems Laboratory (LSI) research group. Educated entirely at UPM (PhD 1999), she enhanced her profile with research stays at prestigious institutions including MIT, UC Berkeley, Bell Laboratories and Politecnico di Torino.

Her research focuses on cutting-edge areas within microelectronics and VLSI design, including low-power and energy-efficient circuits, nanometric technologies (addressing variability, reliability, and radiation effects), reconfigurable computing (FPGAs), emerging memories (RRAM/Memristors), hardware security (PUFs), neuromorphic computing and more recently heterogeneous integration and chiplets.

Professor López Vallejo is highly recognized nationally, holding 5 research sexenios and 1 transfer sexenio. She played influential roles in national science policy as a funding manager for the State Research Agency (AEI) in the ICT-Microelectronics area and is currently a member of the Spanish government's high-level PERTE Chip expert group.

Internationally, her expertise is acknowledged through Editor and Associate Editor positions at top IEEE journals (Transactions on Nanotechnology and TCAS-I) and leadership roles in major conferences (ESSERC, ISLPED, PATMOS, DATE). She has led over 17 R&D projects, including five consecutive national plan grants, authored highly cited publications and three patents. In addition, she successfully supervised numerous PhD students (13), all achieving the highest distinction. Her profile integrates high-impact research, national strategic influence, international community leadership, and successful mentorship.

Part C. RELEVANT MERITS *(sorted by typology)*

C.1. Most important publications (JCR last 5 years)

1. M. Garrido, D. Medina, P. Paz and M. López-Vallejo, "Uniformly Distributed CORDIC," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, doi: 10.1109/TCSI.2025.3560802.
2. B. Gutiérrez de Cabiedes, J. de Mena, A. de Gracia, M. Lopez-Vallejo. “An Ultra-Low-Power Flip-Flop with Near-Threshold Robust Operation and Redundant-Free Internal Clock Transitions". IEEE Trans. on Circuits and Systems I: Regular Papers. 2025. doi: 10.1109/TCSI.2025.3551815.
3. S. López-Asunción, J. González-López, C. García-de-la-Cueva, M. López-Vallejo and J. Grajal, "Design and Implementation of a Real-Time Low-Latency Automatic Modulation Classifier," in *IEEE Transactions on Instrumentation and Measurement*, vol. 74, 2025, doi: 10.1109/TIM.2024.3497146.
4. J de Mena Pacheco, JM Carrillo, T Palacios, M Lopez-Vallejo, “A Highly Power-and Area-Efficient PMU for Cell-Size Autonomous Microsystems” IEEE Trans. Circuits and Systems I, Nov. 2024.
5. L Pistolesi, L Ravelli, A Glukhov, A de Gracia, M Lopez-Vallejo, ... "Differential Phase Change Memory (PCM) Cell for Drift-Compensated In-Memory Computing," in *IEEE Transactions on Electron Devices*, vol. 71, no. 12, pp. 7447-7453, Dec. 2024, doi: 10.1109/TED.2024.3480898.
6. J. de Mena, T Palacios, M Hempel, ML Vallejo, “A Highly Linear Ultra-Low-Area-and-Power CMOS Voltage-Controlled Oscillator for Autonomous Microsystems”, Micromachines 15 (10), 2024.
7. V.M. Bautista, M Garrido, M López-Vallejo, “Serial butterflies for non-power-of-two FFT architectures in 5G and beyond”. IEEE Trans. on Circuits and Systems I. 70 (20) Oct. 2023.
8. M. Molina, J. Mendez, D. P. Morales, E. Castillo, M. López-Vallejo and M. Pegalajar, "Power-Efficient Implementation of Ternary Neural Networks in Edge Devices," IEEE Internet of Things Journal, Dic. 2022.
9. H. Aparicio, P. Ituero, M López-Vallejo, “Reference-free power supply monitor with enhanced robustness against process and temperature variations”, Integration 82, 127-135. 2022.
10. A. de Gracia Herranz, M. Lopez-Vallejo, “Time to digital sensing for multilevel RRAM cells”, IEEE Access 9, 160216-160223, Dec. 2021.
11. A Bahramali, M. Lopez-Vallejo, “An RFID-Based Self-Biased 40 nm Low Power LDO Regulator for IoT Applications” Micromachines 12 (4), 2021
12. A de Gracia Herranz, M. Lopez-Vallejo “Time-domain writing architecture for multilevel RRAM cells resilient to temperature and process variations” Integration 75, 141-149, 2020
13. E Pun-García, M. López-Vallejo, “A Survey of Analog-to-Digital Converters for Operation under Radiation Environments” Electronics 9 (10), 2020
14. X Zhang, J Grajal, M. López-Vallejo, E McVay, T Palacios “Opportunities and Challenges of Ambient Radio-Frequency Energy Harvesting” Vol. 4, Is. 6, 17 June 2020, Pages 1148-1152.
15. A de Gracia Herranz, M Lopez-Vallejo “Time-domain writing architecture for multilevel RRAM cells resilient to temperature and process variations” Integration 75, 141-149, 2020.
16. E Pun-García, M López-Vallejo “A Survey of Analog-to-Digital Converters for Operation under Radiation Environments” Electronics 9 (10), 1694, 2020.

C.2. Projects (from 2010)

Cátedra PERTE Chip UPM-Indra en Microelectrónica (TSI-069100-2023-0016)
Funding agency: Ministerio de de Asuntos Económicos y Transformación Digital, with NextGenerationEU funding
Partners: UPM and INDRA
Duration, from: May 1st 2024 to: June 30th 2027 Budget: 5.025.000,00 Euros
Principle Investigator: Vicerrector de Investigación (UPM)
Technical Director: María Luisa López Vallejo
Number of researchers: 50

PID2022-141391OB-C21: Emerging Technologies and Platforms for Neuromorphic Computing in Space (NEUROSPACEWARE)
Funding agency: Ministerio de Ciencia e Innovación Budget: 200.000€
Partners: Dpto. Ingeniería Electrónica (UPM) y UPC
Duration, from: 1/9/23 to: 31/08/24
Principle Investigator: María Luisa López Vallejo and Pablo Ituero

PDC2022-133657-I00: Sistemas Ultraligeros de Monitorizacion para Vehiculos Aéreos no Tripulados Basados en Redes Neuronales Convolucionales (Neuro-UAV)
Funding agency: AEI, Prueba de Concepto Budget: 137.885€
Partners: Laboratorio de Sistemas Integrados (UPM)
Duration, from: 1/12/22 to: 30/11/24
Principle Investigator: María Luisa López Vallejo y Pablo Ituero

Neuromorphic computing for SatCom Applications
Funding agency: ESA Budget: 350.000€ Dutation: 5/5/22 to 16/3/23
Partners: Dpto. Ingeniería Electrónica (UPM), Thales A. S, University of Manchester.
Project coordinator: María Luisa López Vallejo

MISTI: Autonomous Synthetic Cells for Sensing Applications
Funding agency: MISTI-SPAIN Budget: 25.000$
Partners: Dpto. Ingeniería Electrónica (UPM) y MTL Lab (MIT)
Duration, from: 1/1/20 to: 31/08/21
Principle Investigator: María Luisa López Vallejo (UPM), Tomás Palacios (MIT)

PGC2018-097339: Efficient and Robust Hardware for Brain-Inspired Computing (NEUROWARE)
Funding agency: CICYT Budget: 161.777€
Partners: Dpto. Ingeniería Electrónica (UPM)
Duration, from: 1/1/19 to: 31/12/22
Principle Investigator: María Luisa López Vallejo and Pablo Ituero

TEC2015-65902: Variability in Nanometric technologies: Tolerance, Reliability and Benefits (TOLERA2)
Funding agency: CICYT Budget: 72.100€
Partners: Laboratorio de Sistemas Integrados (UPM)
Duration, from: 1/01/16 to: 31/12/18
Principle Investigator: María Luisa López Vallejo

C.3. Contracts

Title: State of the Art of EDGE AI Components and Technologies
Funding entity: Indra. Duration:15/2/24 a 14/2/25.
Principle Investigator UPM: María Luisa López Vallejo
Budget (UPM): 60.000€

Title: Autonomous sensing platform for structural monitoring of transmission towers. Subcontrato desde MIT, Funding entity: Ferrovial. Duration:1/1/22 - 31/12/23.
Principle Investigator UPM: María Luisa López Vallejo
Budget (UPM): $70.000

Title: Análisis tecnológico y desarrollo de técnicas de mitigación de fallos en la tecnología GF 22FDX
Funding agency: Arquimea Space and Defense. Duración:1/09/2021 to: 30/06/22
Principle Investigator UPM: María Luisa López Vallejo
Budget (UPM): 35.000 Euros

Title: Diseño de módulos de análisis intra-pulso y pulso corto en FPGA
Partners: INDRA S.A. Universidad Politécnica de Madrid (GMR y LSI)
Duration:1/10/2018 to 26/5/2022 Budget : 145.000 Euros
Principal investigator: Jesús Grajal (SSR-UPM), Marisa López Vallejo (LSI-UPM)

C.4. Patents

Inventors: T. Gabara, Inkyu Lee, M. L. López-Vallejo, y S. Mujtaba
Title: Block Processing in a Maximum a Posteriori Processor for Reduced Power Consumption Number: 7353450 Priority Country: USA Date: 1 April 2008 Organization: Agere Systems Inc. Países a los que se ha extendido: EEUU
Under exploitation of: Agere Systems Inc.

Inventors: C. Arrabal, P. Ituero, M. L. López-Vallejo y C. López Barrio
Title: Procedimiento y arquitectura electrónica para la detección SOVA óptima
Number: P200701056 Priority Country: Spain Date: 19/04/2007 Organization: Universidad Politécnica de Madrid

Inventors: P. Ituero, J.L. Ayala Rodrigo, M. L. López-Vallejo
Title: Aparato para la medida de temperatura y corriente de fugas en un chip
Number: P200702109 Priority Country: España, Europa, EEUU
Date: 16/07/2008 Organization: Universidad Politécnica de Madrid

C.5 PhD supervision: 9 in the last 10 años

- "Design of Ultra-Low Power and Area Circuits for Cell-Size Microsystems" J. de Mena, Jan. 2025
- "Contribution to the Design and Implementation of Rad-Hard ΣΔ Analog-to-Digital Converters. E. Pun, 8 Feb. 2024
- "Interfacing memristors for reliable computing". Amadeo de Gracia, 20 Diciembre 2023.
- "Variability-aware design of front-end circuits for self-powered applications". Asghar Bahramali 24 Mayo 2021.
- "Resistive RAM: Simulation and Modeling for Reliable Design". Fernando García Redondo, 5 de junio de 2017
- "Study, design and validation of a framework model for smoke and particle-filled atmospheres". José María Nadal Serrano, 27 de abril de 2017
- "Modeling and Design of Ring Oscillators and their Applications in Radiation Environments". Javier Agustín Sáenz, 16 marzo de 2017
- "Fault management techniques for systems with SRAM-based FPGAs", Ignacio Herrera Alzu. 23 de julio de 2015
- "Design and simulation of deep nanometer SRAM cells under energy, mismatch, and radiation constraints" Pablo Royer del Barrio. 22 de julio de 2015

C.6 Participation in evaluation processes: CICYT, ANEP, EU

C.7 Member of Tecnical Program Committees and Editorial boards (last 10 years)

- IEEE trans. on Circuits and Systems I, associate editor from January 2024.
- IEEE trans. on Nanotechnology, Editor desde 2023. Associate editor from 2017 to 2023.
- PATMOS 2018, General Chair. PATMOS 2019, Program Chair.
- Design Automation and Conference (DATE). Executive Committee, 2017, 2020, 2021.
- ISLPED 2019 - 2024 Program Committee.
- DATE Program Committee. Editions: 2010 - 2015 and 2016.
- IEEE ESSCIRC / ESSER Program Committee. Editions: 2023 and 2024.
- Greal Lake Symposium on VLSI (GLSVLSI). Editions: 2011 – 2016.
- From 2008 member of the Steering Committee del Design of Circuits and Integrated Systems (DCIS). General Chair in 2020.

C.8 Management responsiblities

- From April 2020 to Feb. 2024 Manager of the TIC-MNF area at the Agencia Estatal de Investigación.
- Subdirectora para Planificación y Ordenación Académica en la E.T.S.I. Teleco-municación (UPM) from January 2013 to July 2015.